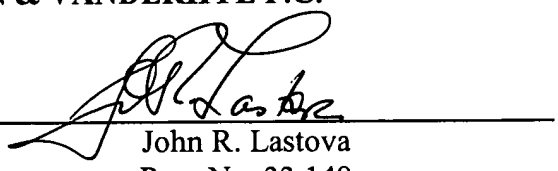
Markis's approach is quite different from what is claimed where arbitration between memory access requests from a memory access interface portion and a processing portion is performed. The present application seeks to address a potential problem that arises when a memory access interface needs to transfer a lot of data and therefore has sole use of a bus for a significant length of time thereby having a significant effect on processor performance. The problem is solved using multiple dedicated buses and arbitration logic associated with a read/write port which routes the different memory portion access requests to the appropriate dedicated bus.

The secondary Tamura reference does not overcome the deficiencies noted above with respect to Markis. Accordingly, the application is in condition for allowance. An early notice to that effect is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
John R. Lastova
Reg. No. 33,149

JRL:maa
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100